Marshall Space Flight Center will be a part of a larger system that will process the IC's from start to finish with minimal human intervention. A number of carriers will be used to transport the chips from one station to another, eliminating the damage that occurs from manual handling. The facility will produce ultrareliable IC's that will last 25 years or longer in spaceflights and other critical applications.

The reported facility consists of an automatic scrubber, photoresist coater and developer, mask aliner, IR (infrared) bake, and inspection stations. The heart of the facility is the wafer carrier system. Four distinct carriers are utilized, depending on the nature of wafer processing. There is a standard aluminum carrier for all regular operations, a polypropylene carrier for areas with chemical solutions and caustic agents, quartz boats for high-temperature environments, and an inverting carrier for flip-transferring the wafers from one carrier system to another. Each carrier can handle 25 wafers at a time, the wafer diameter being 3 in. (7.5 cm).

An automatic in-line scrubber cleans the wafers with high-speed brush and solvent prior to other processing. This program-controlled station scrubs the wafers without creating mechanical stresses.

A single-head photoresist-coater and developer station is program-controlled and may include nitrogen purge, a spray wash, spin drying, precoating, and photoresist coating in its photoresist-coating cycle. A develop cycle may include various solvent washes and developer rinses with spin drying.

The automatic mask-aliner station alines the mask with the wafers using an optical-scanning computer control. The alined wafers are exposed to ultraviolet light for printing the pattern on the wafers and are then fed to the developer station.

The hard-bake IR station processes the coated wafers in 1 to 4 min and in 4 to 7 min after developing. The station includes a nitrogen purge available from two built-in nozzles.

The inspection station equipped with a micromanipulator includes a microscope to examine the wafers under low and high magnifications. A pantograph with template is also available for quick inspection. Acceptable wafers are returned to the wafer carrier by foot-switch command, while the rejects are sent to a holding position.

The report includes a number of illustrations showing various optical schemes for detecting and alining the chips. Photographs of the facility are also included.

This work was done by Bobby W. Kennedy of **Marshall Space Flight Center.** *To obtain a copy of the report, "Photolithography for Automatic Processing of Integrated Circuits," Circle 80 on the TSP Request Card.*
MFS-25073

Models of MOS and SOS Devices

A report on progress in the processing of metal-oxide-semiconductor and silicon-on-sapphire IC's

A quarterly report on trends and techniques for space-base electronics describes progress in three programs:

1. The development of a dc sputtering machine for aluminum and aluminum alloys,
2. The development of two-dimensional computer models of metal-oxide-semiconductor (MOS) transistors, and
3. The development of a computer program for calculating the redistribution diffusion of dopants in silicon-on-sapphire (SOS) films.

The sputtering machine can accommodate eight wafers for aluminum deposition. It rotates the wafers through three sputter-gun positions and two mask positions. The sputtering chamber opens into a clean bench located in a clean room.

The finite-element method of analysis was investigated as a means of modeling MOS transistors. Although the finite-element method is reportedly convenient in treating nonrectangular geometries and irregular boundaries, it produced disappointing results in the study; its accuracy was no better than that of the finite-difference method.

An MOS algorithm has been developed on the assumption that mobile carriers are included in an infinitesimally thin layer of charge at the silicon/silicon dioxide interface. The algorithm proceeds in an iterative fashion to solve simultaneously a one-dimensional current equation and Poisson's equation. The solution yields the potential distribution from which current is calculated as a function of the gate, drain, and body voltages.

The MOS model as it stands neglects generation/recombination mechanisms and therefore cannot treat impact-avalanche and bulk-generated leakage currents. However, it is likely that such effects can be treated by adding another iterative loop to the algorithm.

The SOS redistribution diffusion computer program is intended to produce curves showing the effects of diffusion time and temperature on junction depth, sheet resistance, and integrated ion-implanted impurity dose. These data have been generated for boron and phosphorus redistribution in nitrogen, dry oxygen, and steam ambients for SOS films in ⟨111⟩ crystal orientation. (The report furnishes the data in an appendix.)

The program contains three basic mathematical models: (1) an implantation profile, (2) an oxidation model, and (3) a diffusivity model. It was developed to account for both thin and thick oxides, but at present is limited to thin oxides because the simulation of both thick and thin oxides requires that a warped grid system be incorporated in the program — a modification that would demand considerable additional effort.

This work was done by J. D. Gassaway, Q. Mahmood, and J. D. Trotter of Mississippi State University for **Marshall Space Flight Center.** *To obtain a copy of the report, "Trends and Techniques for Space Base Electronics," Circle 81 on the TSP Request Card.*
MFS-25153